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- A voltage regulator having an input terminal and an output terminal, comprising:
- a first transistor connecting the input terminal to an intermediate terminal;
- a second transistor connecting the intermediate terminal to ground;
- a controller that drives the first and second transistors to alternately couple the intermediate terminal between the input terminal and ground, wherein the controller drives the first transistor with a first gate voltage and drives the second transistor with a second, different gate voltage; and
- a filter disposed between the input terminal and the output terminal to provide a substantially DC voltage at the output terminal, the filter including at least one element connecting the intermediate terminal to the output terminal.
- 2. The voltage regulator of claim 1, wherein the first transistor is a PMOS transistor and the second transistor is an NMOS transistor.
- 3. The voltage regulator of claim 2, wherein the first voltage is larger than the second voltage.
- 4. The voltage regulator of claim 3, wherein the first voltage is substantially equal to an input voltage at the input terminal.
- 5. The voltage regulator of claim 3, wherein the second gate voltage is compatible with a logic voltage.
- 25 6. The voltage regulator of claim 5, wherein the first gate voltage is greater than the logic voltage.
 - 7. The voltage regulator of claim 3, wherein the first transistor includes a first gate oxide layer, the second transistor includes a second gate oxide layer, and the first gate oxide layer is thicker than the second gate oxide layer.

- 8. The voltage regulator of claim 1, wherein the controller includes a first plurality of transistors in a drive train of the first transistor and a second plurality of transistors in a drive train of the second transistor.
- 5 9. The voltage regulator of claim 8, wherein the second plurality of transistors are driven with the second gate voltage.
 - 10. The voltage regulator of claim 8, wherein the first plurality of transistors includes a third transistor driven with the first gate voltage and a fourth transistor driven with the second gate voltage.

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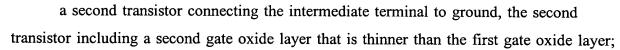
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- A voltage regulator having an input terminal and an output terminal, comprising:
 a transistor to intermittently couple the input terminal to the output terminal, wherein
 the transistor includes a source, a drain, and a gate, and the transistor has a channel length
 between the source and the drain which is less than a channel length required for reliable
 behavior under steady state saturation conditions; and
- a filter disposed between the input terminal and the output terminal to provide a substantially DC voltage at the output terminal.
- 12. The voltage regulator of claim 11, wherein the channel length is about 1 micron.
- 13. The voltage regulator of claim 11, wherein the channel length is shorter than a channel length specified for standard hot electron specification of 10% degradation in a one year period of operation.
- 14. The voltage regulator of claim 11, wherein the transistor is fabricated using one or more of process proximity correction and phase shift mask technology.
- 18. A voltage regulator having an input terminal and an output terminal, comprising:
 a first transistor connecting the input terminal to an intermediate terminal, the first transistor including a first gate oxide layer;

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a controller that drives the first and second transistors to alternately couple the intermediate terminal between the input terminal and ground; and

a filter disposed between the input terminal and the output terminal to provide a substantially DC voltage at the output terminal, the filter including at least one element connecting the intermediate terminal to the output terminal.

The voltage regulator of claim 1/5, wherein the first transistor is a PMOS transistor and the second transistor is an NMOS transistor.

12 17. The voltage regulator of claim 16, wherein the controller drives the first transistor with a first gate voltage and drives the second transistor with a second, different gate voltage.

14. 18. The voltage regulator of claim 1/2, wherein the first voltage is larger than the second voltage.